Claims

What is claimed is:

1. A symbol synchronizer for a software-defined communications system diversity receiver, comprising:

a single matched filter for filtering an input digital signal with a match filtering function based on predetermined signal transfer function characteristics;

a signal delay bank including a plurality of delay blocks each for delaying the input digital signal filtered by the single matched filter for a predetermined number of samples;

a complex correlator for correlating the input digital signal filtered by the single matched filter and delayed by the signal delay bank with a correlator reference signal, and for selecting an index of a path having a peak correlator value.

2. The symbol synchronizer of claim 1, wherein the single matched filter comprises a single complex sliding window matched filter for providing a sliding estimate of a predetermined number of most recent samples of the input digital signal.

3. The symbol synchronizer of claim 2, wherein the complex sliding window matched filter has an input/output relationship expressed mathematically as:

$$CSWMF(n) = \xi CSWMF(n-1) + (1/N)(\alpha x(n) - \gamma x(n-N)),$$

where CSWMF(n) is an output of the complex sliding window matched filter at time n, ξ is a complex valued filter tap weight vector, α and γ are respective complex valued tap weights, x(n) is an input to the complex sliding window matched filter at time (n), and N is a filter length of the complex sliding window matched filter.

4. The symbol synchronizer of claim 2, wherein the complex sliding window matched filter is for directly estimating symbol synchronization.

5. The symbol synchronizer of claim 1, wherein the complex correlator is for correlating the input digital signal filtered by the single matched filter and delayed by the signal delay bank with a correlator reference signal that is a correlation estimator.

6. The symbol synchronizer of claim 1, wherein the complex correlator is executed only at zero lag for correlating the input digital signal with a correlator reference signal that is a complex average power measurement of an output of the single matched filter.

7. The symbol synchronizer of claim 4, wherein the complex correlator is for correlating the input digital signal filtered by the single complex sliding window matched filter and delayed by the signal delay bank with a correlator reference signal having a known reference pattern.

8. The symbol synchronizer of claim 7, wherein the complex correlator is for selecting the index of a path having a peak correlator value through a correlator maximum value block.

9. The symbol synchronizer of claim 8, wherein the correlator maximum value block is for averaging the input digital signal filtered by the single complex sliding window matched filter and delayed by the signal delay bank over a predetermined number of symbols.

10. The symbol synchronizer of claim 9, wherein the predetermined number of symbols is 16.

11. The symbol synchronizer of claim 1, wherein the single matched filter is first downsampled by a factor N equal to a number of samples per symbol, and wherein subsequent samples are then operated on by determining a complex average power.

12. A diversity signal combiner system for a digital communications system, comprising:

a plurality of channels each for receiving a channel signal of a plurality of channel signals from a spatially diverse antenna array element;

a plurality of downconverters each on one of the plurality of channels for downconverting a corresponding channel signal to baseband;

a co-phasing software block for resolving phase differences among the plurality of channel signals after the plurality of channel signals are downconverted by the plurality of downconverters;

a combiner for combining the plurality of channel signals by weighting and delaying each of the plurality of channel signals after the co-phasing software block resolves the phase differences among the plurality of channel signals; and

a symbol synchronizer for determining symbol boundaries of the plurality of channel signals after the combiner combines the plurality of channel signals to enable a system signal to be accurately demodulated to accurately represent transmitted data.

13. The diversity signal combiner system of claim 12, wherein the symbol synchronizer includes a single complex sliding window matched filter for filtering the plurality of channel signals with a match filtering function based on predetermined signal transfer function characteristics to average noise out of the plurality of channel signals and thereby maximize a signal-to-noise ratio of each of the plurality of channel signals.

14. The diversity signal combiner system of claim 13, further comprising an equalizer for receiving the plurality of channel signals from the combiner, for providing channel estimates of complex channel gain when necessary, and for removing channel effects from the plurality of channel signals before the plurality of channel signals are input into the single complex sliding window matched filter.

15. The diversity signal combiner system of claim 14, wherein the symbol synchronizer is for providing a variable step size parameter to the equalizer according to a confidence measure of correct symbol boundary estimation.

16. The diversity signal combiner system of claim 14, further comprising an adaptive weight, delay and phase updater connected between the combiner and the equalizer for estimating and correcting phase gain, frequency and sampling error effects, and for receiving

feedback from the single complex sliding window matched filter and the symbol synchronizer for providing a variable step size parameter, and fast error convergence, in the equalizer.

17. The diversity signal combiner system of claim 16, wherein the equalizer is connected to the adaptive weight, delay and phase updater via a feedback loop to accept a new value of the variable step size parameter and to return a combined channel signal estimate to the adaptive weight, delay and phase updater.

18. The diversity signal combiner system of claim 13, wherein the single complex sliding window matched filter is connected to the symbol synchronizer via a closed feedback loop to provide a variable step size for fast delay, channel and phase estimate convergence performance.

19. A diversity signal combiner system for a digital communications system, comprising:

a plurality of channels each for receiving a signal from a spatially diverse antenna array element;

a plurality of downconverters each on one of the plurality of channels for downconverting a corresponding plurality of channel signals to baseband;

a plurality of matched filters each being located on one of the plurality of channels for filtering the corresponding plurality of channel signals with a match filtering function based on predetermined signal transfer function characteristics to average noise out of the

corresponding plurality of channel signals to maximize a signal-to-noise ratio of each of the plurality of channel signals;

a combiner for combining each of the plurality of channel signals output from the plurality of matched filters by appropriately weighting and delaying each of the plurality of channel signals; and

a symbol synchronizer for determining symbol boundaries of the plurality of channel signals output from the plurality of matched filters as the combiner weights and delays each of the plurality of channel signals, thereby causing a single combined signal with digital sampling to be output from the combiner.

20. The diversity signal combiner system of claim 19, further comprising an adaptive delay/phase updater for receiving digitally sampled signals from a variable delay in each of the plurality of channels.

21. The diversity signal combiner system of claim 20, further comprising an equalizer for generating a signal phase/delay estimation error and for inputting the signal phase/delay estimation error into the adaptive phase/delay updater;

wherein the symbol synchronizer is further for generating a confidence measure and inputting the confidence measure into the adaptive phase/delay updater; and

wherein the adaptive phase/delay updater measures and updates the signal phase/delay estimation error based on the confidence measure.

22. The diversity signal combiner system of claim 20, wherein the adaptive phase/delay updater is connected to each of the plurality of downconverters via respective output vector lines for adjusting respective downconverter oscillator sampling frequencies and sampling phases, and for providing a delay in each of the plurality of channels.

23. The diversity signal combiner system of claim 19, further comprising an equalizer for receiving the combined channel signals from the combiner and for providing combiner weight updating on the plurality of channel signals.

24. The diversity signal combiner system of claim 23, further comprising a sampling time update block for executing a sampling time update equation and for outputting results of the executed sampling time update equation to the plurality of downconverters to control a sampling time of the plurality of channel signals input to the plurality of downconverters.

25. The diversity signal combiner system of claim 24, wherein the symbol synchronizer is further for providing confidence measures to both the equalizer and the sampling time update block to provide adjustable step size in both the sampling time update block and the equalizer.

26. The diversity signal combiner system of claim 23, wherein the equalizer further includes a vector input line for accepting output samples from the plurality of matched filters, the equalizer further for estimating a complex channel gain for each of the plurality of channels based on the accepted output samples.

27. The diversity signal combiner system of claim 26, wherein the equalizer is further for generating a weight vector output for correcting channel complex gain errors.

28. The diversity signal combiner system of claim 23, wherein the symbol synchronizer is further for adaptively updating a convergence rate of the equalizer.

29. The diversity signal combiner system of claim 23, wherein the symbol synchronizer is further for providing a control signal to the equalizer for providing optimal sampling at an output of the equalizer to minimize a demodulated data bit error rate.